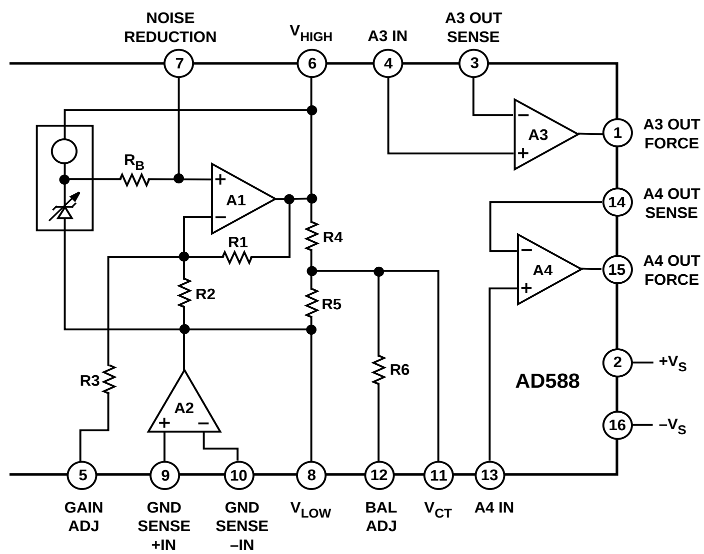
High Precision Voltage Reference

AD588*

FEATURES
Low Drift: 1.5 ppm/°C
Low Initial Error: 1 mV
Pin-Programmable Output
+10 V, +5 V, ±5 V Tracking, –5 V, –10 V
Flexible Output Force and Sense Terminals
High Impedance Ground Sense
Machine-Insertable DIP Packaging
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD588 represents a major advance in the state-of-the-art in monolithic voltage references. Low initial error and low temperature drift give the AD588 absolute accuracy performance previously not available in monolithic form. The AD588 uses a proprietary ion-implanted buried Zener diode, and laser-wafer-drift trimming of high stability thin-film resistors to provide outstanding performance at low cost.

The AD588 includes the basic reference cell and three additional amplifiers which provide pin-programmable output ranges. The amplifiers are laser-trimmed for low offset and low drift to maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high-current loads, delivering the full accuracy of the AD588 where it is required in the application circuit.

The low initial error allows the AD588 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD588 can provide a known voltage for system calibration in software and the low drift allows compensation for the drift of other components in a system. Manual system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD588 in conjunction autocalibration software.

The AD588 is available in seven versions. The AD588 JQ and KQ grades are packaged in a 16-pin cerdip and are specified for 0°C to +70°C operation. AD588AQ and BQ grades are packaged in a 16-pin cerdip and are specified for the –25°C to +85°C industrial temperature range. The ceramic AD588SQ and TQ grades are specified for the full military/aerospace temperature range. For military surface mount applications, the AD588SE and TE grades are also available in 20-pin LCC packages.

***Covered by Patent Number 4,644,253.**

PRODUCT HIGHLIGHTS

1. The AD588 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the Zener or the buffer amplifiers and thus does not increase the temperature drift.
2. Output noise of the AD588 is very low—typically 6 μV p-p. A pin is provided for additional noise filtering using an external capacitor.
3. A precision ±5 V tracking mode with Kelvin output connections is available with no external components. Tracking error is less than one millivolt and a fine-trim is available for applications requiring exact symmetry between the +5 V and –5 V outputs.
4. Pin strapping capability allows configuration of a wide variety of outputs: ±5 V, +5 V and +10 V, –5 V & –10 V dual outputs or +5 V, –5 V, +10 V, –10 V single outputs.
5. Extensive temperature testing at –55°C, –25°C, 0°C, +25°C, +50°C, +70°C, +85°C and +125°C ensures that the specified temperature coefficient is truly representative of device performance.

REV. B

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AD588–SPECIFICATIONS (typical @ + 25°C, +10 V output, V_S = ±15 V unless otherwise noted[1])

	AD588SQ			AD588JQ/AQ/TQ			AD588KQ/BQ			
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
OUTPUT VOLTAGE ERROR										
+10 V, –10 V Outputs	**–5**		**+5**	**–3**		**+3**	**–1**		**+1**	mV
+5 V, –5 V Outputs	**–5**		**+5**	**–3**		**+3**	**–1**		**+1**	mV
±5 V TRACKING MODE										
Symmetry Error	**–1.5**		**+1.5**	**–1.5**		**+1.5**	**–0.75**		**+0.75**	mV
OUTPUT VOLTAGE DRIFT										
0°C to +70°C (J, K, B)				**–3**	±2	**+3**	**–1.5**		**+1.5**	ppm/°C
–25°C to +85°C (A, B)				**–3**		**+3**	**–3**		**+3**	ppm/°C
–55°C to +125°C (S, T)	**–6**		**+6**	**–4**		**+4**				ppm/°C
GAIN ADJ AND BAL ADJ[2]										
Trim Range		±4			±4			±4		mV
Input Resistance		150			150			150		kΩ
LINE REGULATION										
T_{MIN} to T_{MAX}[3]			**±200**			**±200**			**±200**	µV/V
LOAD REGULATION										
T_{MIN} to T_{MAX}										
+10 V Output, 0 < I_{OUT} < 10 mA			**±50**			**±50**			**±50**	µV/mA
–10 V Output, –10 < I_{OUT} < 0 mA			**±50**			**±50**			**±50**	µV/mA
SUPPLY CURRENT										
T_{MIN} to T_{MAX}		6	**10**		6	**10**		6	**10**	mA
Power Dissipation		180	**300**		180	**300**		180	**300**	mW
OUTPUT NOISE (Any Output)										
0.1 Hz to 10 Hz		6			6			6		µV p-p
Spectral Density, 100 Hz		100			100			100		nV/$\sqrt{Hz}$
LONG-TERM STABILITY (@ +25°C)		15			15			15		ppm/1000 hr
BUFFER AMPLIFIERS										
Offset Voltage		100			100			10		µV
Offset Voltage Drift		1			1			1		µV/°C
Bias Current		20			20			20		nA
Open Loop Gain		110			110			110		dB
Output Current A3, A4	–10		+10	–10		+10	–10		+10	mA
Common-Mode Rejection (A3, A4)										
V_{CM} = 1 V p-p		100			100			100		dB
Short-Circuit Current		50			50			50		mA
TEMPERATURE RANGE										
Specified Performance										
J, K Grades				0		+70	0		+70	°C
A, B Grades				–25		+85	–25		+85	°C
S, T Grades	–55		+125	–55		+125				°C

NOTES

[1]Output — Configuration
+10 V — Figure 2a
–10 V — Figure 2c
+5 V, –5 V, ±5 V — Figure 2b

Specifications tested using +10 V configuration unless otherwise indicated.

[2]Gain and balance adjustments guaranteed capable of trimming output voltage error and symmetry error to zero.

[3]Test Conditions:
+10 V Output — $-V_S$ = –15 V, 13.5 V ≤ $+V_S$ ≤ 18 V
–10 V Output — –18 V ≤ $-V_S$ ≤ –13.5 V, $+V_S$ = 15 V
±5 V Output — $+V_S$ = +18 V, $-V_S$ = –18 V
$+V_S$ = +10.8 V, $-V_S$ = –10.8 V

Specifications subject to change without notice

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ORDERING GUIDE

Part Number[1]	Initial Error	Temperature Coefficient	Temperature Range °C	Package Option
AD588AQ	3 mV	3 ppm/°C	–25 to +85	Cerdip (Q-16)
AD588BQ	1 mV	1.5 ppm/°C	–25 to +85[2]	Cerdip (Q-16)
AD588SQ	5 mV	6 ppm/°C	–55 to +125	Cerdip (Q-16)
AD588TQ	3 mV	4 ppm/°C	–55 to +125	Cerdip (Q-16)
AD588JQ	3 mV	3 ppm/°C	0 to +70	Cerdip (Q-16)
AD588KQ	1 mV	1.5 ppm/°C	0 to +70	Cerdip (Q-16)

NOTES

[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD588/883B.

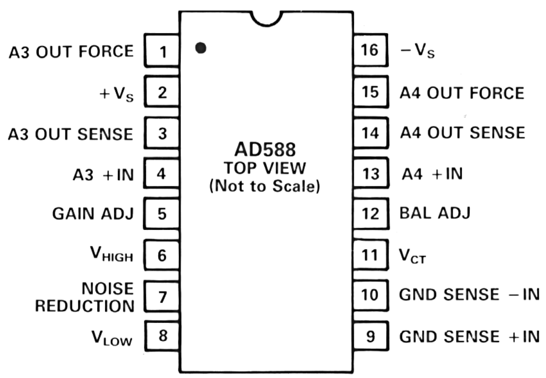
[2]Temperature coefficient specified from 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to $–V_S$ . . . . 36 V
Power Dissipation (+25°C)
Q Package . . . . 600 mW
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . +300°C
Package Thermal Resistance
Q (θ_{JA}/θ_{JC}) . . . . 90/25°C/W
Output Protection: All Outputs Safe If Shorted to Ground

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS



THEORY OF OPERATION

The AD588 consists of a buried Zener diode reference, amplifiers used to provide pin programmable output ranges, and associated thin-film resistors as shown in the block diagram of Figure 1. The temperature compensation circuitry provides the device with a temperature coefficient of 1.5 ppm/°C or less.

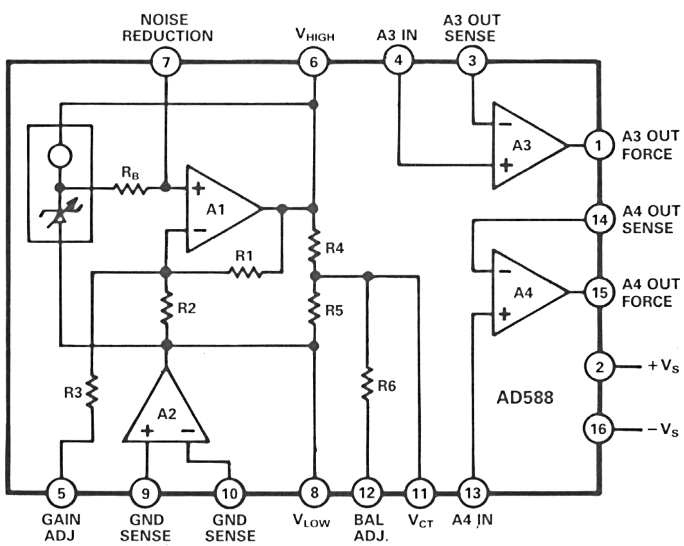


Figure 1. AD588 Functional Block Diagram

Amplifier A1 performs several functions. A1 primarily acts to amplify the Zener voltage from 6.5 V to the required 10 V output. In addition, A1 also provides for external adjustment of the 10 V output through Pin 5, the GAIN ADJUST. Using the bias compensation resistor between the Zener output and the noninverting input to A1, a capacitor can be added at the NOISE REDUCTION pin (Pin 7) to form a low-pass filter and reduce the noise contribution of the Zener to the circuit. Two matched 10 kΩ nominal thin-film resistors (R4 and R5) divide the 10 V output in half. Pin V_{CT} (Pin 11) provides access to the center of the voltage span and Pin 12 (BALANCE ADJUST) can be used for fine adjustment of this division.

Ground sensing for the circuit is provided by amplifier A2. The noninverting input (Pin 9) senses the system ground which will be transferred to the point on the circuit where the inverting input (Pin 10) is connected. This may be Pin 6, 8 or 11. The output of A2 drives Pin 8 to the appropriate voltage. Thus, if Pin 10 is connected to Pin 8, the V_{LOW} pin will be the same voltage as the system ground. Alternatively, if Pin 10 is connected to the V_{CT} pin, it will be ground and Pin 6 and Pin 8 will be +5 V and –5 V respectively.

Amplifiers A3 and A4 are internally compensated and are used to buffer the voltages at Pins 6, 8, and 11 as well as to provide a full Kelvin output. Thus, the AD588 has a full Kelvin capability by providing the means to sense a system ground and provide forced and sensed outputs referenced to that ground.

APPLYING THE AD588

The AD588 can be configured to provide +10 V and –10 V reference outputs as shown in Figures 2a and 2c respectively. It can also be used to provide +5 V, –5 V or a ±5 V tracking reference as shown in Figure 2b. Table I details the appropriate pin connections for each output range. In each case, Pin 9 is connected to system ground and power is applied to Pins 2 and 16.

The architecture of the AD588 provides ground sense and uncommitted output buffer amplifiers which offer the user a great deal of functional flexibility. The AD588 is specified and tested in the configurations shown in Figure 2. The user may choose to take advantage of the many other configuration options available with the AD588. However, performance in these configurations is not guaranteed to meet the extremely stringent data sheet specifications.

As indicated in Table I, a +5 V buffered output can be provided using amplifier A4 in the +10 V configuration (Figure 2a). A –5 V buffered output can be provided using amplifier A3 in the –10 V configuration (Figure 2c). Specifications are not guaranteed for the +5 V or –5 V outputs in these configurations. Performance will be similar to that specified for the +10 V or –10 V outputs.

As indicated in Table I, unbuffered outputs are available at Pins 6, 8 and 11. Loading of these unbuffered outputs will impair circuit performance.

Amplifiers A3 and A4 can be used interchangeably. However, the AD588 is tested (and the specifications are guaranteed) with the amplifiers connected as indicated in Figure 2 and Table I. When either A3 or A4 is unused, its output force and sense pins should be connected and the input tied to ground.

Two outputs of the same voltage may be obtained by connecting both A3 and A4 to the appropriate unbuffered output on Pins 6, 8 or 11. Performance in these dual output configurations will typically meet data sheet specifications.

CALIBRATION

Generally, the AD588 will meet the requirements of a precision system without additional adjustment. Initial output voltage error of 1 mV and output noise specs of 10 µV p-p allow for

Table I. AD588 Connections

Range	Connect Pin 10 To Pin:	Unbuffered[1] Output on Pins –10 V	–5 V	0 V	+5 V	+10 V	Buffered Output Connections	Buffered Output on Pins –10 V	–5 V	0 V	+5 V	+10 V
+10 V	8	–	–	8	11	6	11–13 & 14–15 6–4 & 3–1	– –	– –	– –	15 –	– 1
–5 V or +5 V	11	–	18	11	6	–	8–13 & 14–15 6–4 & 3–1	– –	15 –	– –	– 1	–
–10 V	6	8	11	6	–	–	8–13 & 14–15 11–4 & 3–1	– 1	15 –	– –	– –	– –
+5 V	11	–	–	–	6	–	6–4 & 3–1	–	–	–	1	–
–5 V		–	8	–	–	–	8–13 & 14–15	–	15	–	–	–

[1]"Unbuffered" outputs should not be loaded.

accuracies of 12–16 bits. However, in applications where an even greater level of accuracy is required, additional calibration may be called for. Provision for trimming has been made through the use of the GAIN ADJUST and BALANCE ADJUST pins (Pins 5 and 12 respectively).

The AD588 provides a precision 10 V span with a center tap (V_{CT}) which is used with the buffer and ground sense amplifiers to achieve the voltage output configurations in Table I. GAIN ADJUST and BALANCE ADJUST can be used in any of these configurations to trim the magnitude of the span voltage and the position of the center tap within the span. The GAIN ADJUST should be performed first. Although the trims are not interactive within the device, the GAIN trim will move the BALANCE trim point as it changes the magnitude of the span.

Figure 2b shows GAIN and BALANCE trims in a +5 V and –5 V tracking configuration. A 100 kΩ 20-turn potentiometer is used for each trim. The potentiometer for GAIN trim is connected between Pins 6 (V_{HIGH}) and 8 (V_{LOW}) with the wiper connected to Pin 5 (GAIN ADJ). The potentiometer is adjusted to produce exactly 10 V between Pins 1 and 15, the amplifier outputs. The BALANCE potentiometer, also connected between Pins 6 and 8 with the wiper to Pin 12 (BAL ADJ), is then adjusted to center the span from +5 V to –5 V.

Trimming in other configurations works in exactly the same manner. When producing +10 V and +5 V, GAIN ADJ is used to trim +10 V and BAL ADJ is used to trim +5 V. In the –10 V and –5 V configuration, GAIN ADJ is again used to trim the magnitude of the span, –10 V, while BAL ADJ is used to trim the center tap, –5 V.

In single output configurations, GAIN ADJ is used to trim outputs utilizing the full span (+10 V or –10 V) while BAL ADJ is used to trim outputs using half the span (+5 V or –5 V).

Input impedance on both the GAIN ADJUST and BALANCE ADJUST pins is approximately 150 kΩ. The GAIN ADJUST trim network effectively attenuates the 10 V across the trim potentiometer by a factor of about 1500 to provide a trim range of –3.5 mV to +7.5 mV with a resolution of approximately 550 µV/turn (20 turn potentiometer). The BALANCE ADJUST trim network attenuates the trim voltage by a factor of about 1400, providing a trim range of ±4.5 mV with resolution of 450 µV/turn.

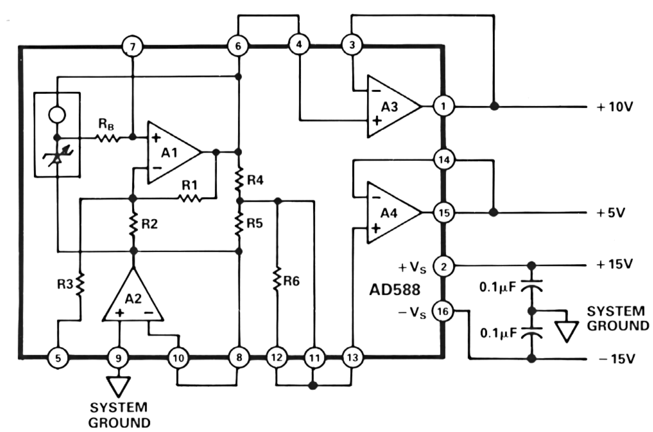


Figure 2a. +10 V Output

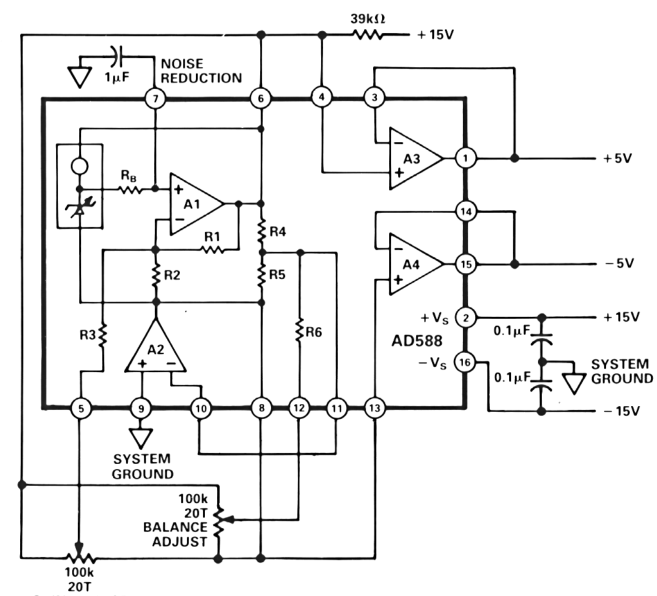


Figure 2b. +5 V and –5 V Outputs

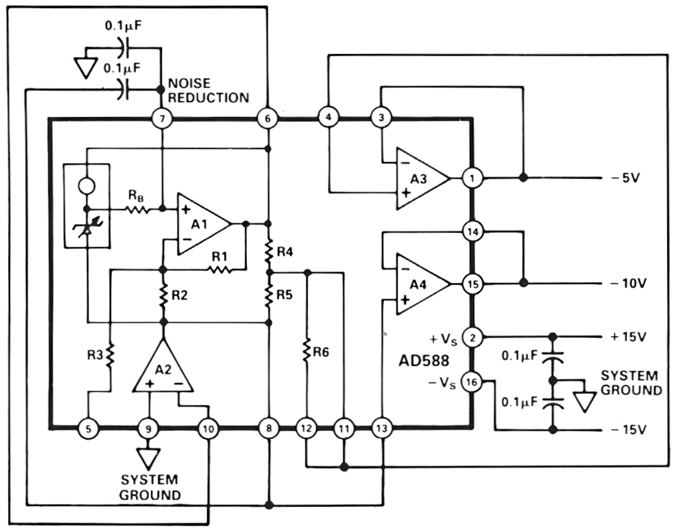


Figure 2c. –10 V Output

Trimming the AD588 introduces no additional errors over temperature so precision potentiometers are not required.

For single output voltage ranges, or in cases when BALANCE ADJUST is not required, Pin 12 should be connected to Pin 11. If GAIN ADJUST is not required, Pin 5 should be left floating.

NOISE PERFORMANCE AND REDUCTION

The noise generated by the AD588 is typically less than 6 µV p-p over the 0.1 Hz to 10 Hz band. Noise in a 1 MHz bandwidth is approximately 600 µV p-p. The dominant source of this noise is the buried Zener which contributes approximately 100 nV/$\sqrt{Hz}$. In comparison, the op amp's contribution is negligible. Figure 3 shows the 0. 1 Hz to 10 Hz noise of a typical AD588.

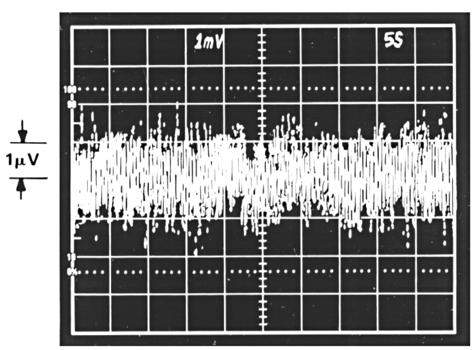


Figure 3. 0.1 Hz to 10 Hz Noise

If further noise reduction is desired, an optional capacitor may be added between the NOISE REDUCTION pin and ground as shown in Figure 2b. This will form a low-pass filter with the 4 kΩ R_B on the output of the Zener cell. A 1 µF capacitor will have a 3 dB point at 40 Hz and will reduce the high frequency (to 1 MHz) noise to about 200 µV p-p. Figure 4 shows the 1 MHz noise of a typical AD588 both with and without a 1 µF capacitor.

Note that a second capacitor is needed in order to implement the NOISE REDUCTION feature when using the AD588 in the –10 V mode (Figure 2c.). The NOISE REDUCTION capacitor is limited to 0.1 µF maximum in this mode.

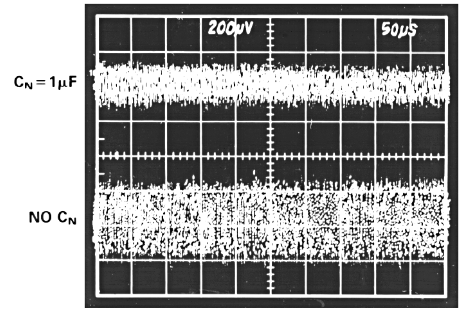
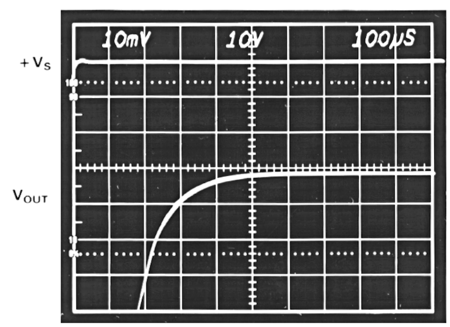


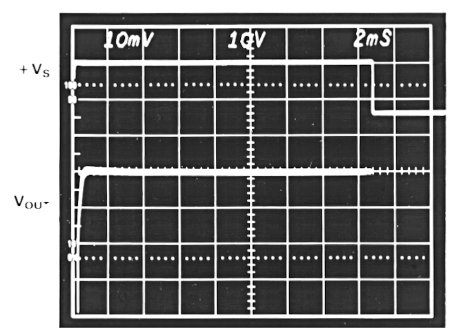
Figure 4. Effect of 1 µF Noise Reduction Capacitor on Broadband Noise

TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is the turn-on settling time. Two components normally associated with this are: time for active circuits to settle and time for thermal gradients on the chip to stabilize. Figure 5 shows the turn-on characteristics of the AD588. It shows the settling to be about 600 µs. Note the absence of any thermal tails when the horizontal scale is expanded to 2 ms/cm in Figure 5b.



a. Electrical Turn-On



b. Extended Time Scale
Figure 5. Turn-On Characteristics

Output turn-on time is modified when an external noise reduction capacitor is used. When present, this capacitor presents an additional load to the internal Zener diode's current source, resulting in a somewhat longer turn-on time. In the case of a 1 µF capacitor, the initial turn-on time is approximately 60 ms (see Figure 6).

Note: If the NOISE REDUCTION feature is used in the ±5 V configuration, a 39 kΩ resistor between Pins 6 and 2 is required for proper start up.

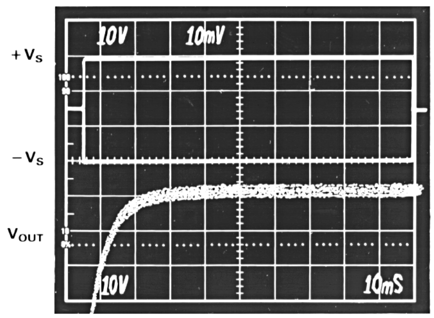


Figure 6. Turn-On with 1 µF C_N

TEMPERATURE PERFORMANCE

The AD588 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Figure 7 shows typical output voltage drift for the AD588BD and illustrates the test methodology. The box in Figure 7 is bounded on the sides by the operating temperature extremes and on top and bottom by the maximum and minimum output voltages measured over the operating temperature range. The slope of the diagonal drawn from the lower left corner of the box determines the performance grade of the device.

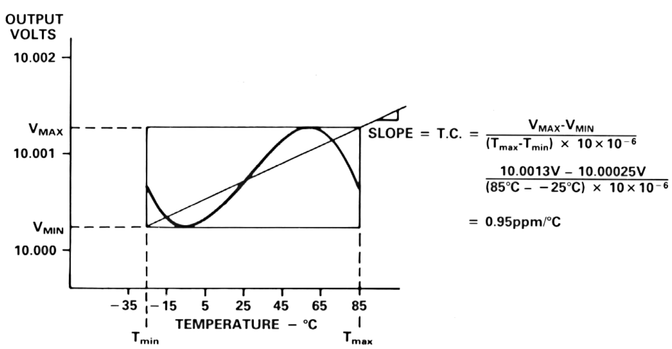


Figure 7. Typical AD588BD Temperature Drift

Each AD588A and B grade unit is tested at –25°C, 0°C, +25°C, +50°C, +70°C and +85°C. Each AD588S and T grade unit is tested at –55°C, –25°C, 0°C, +25°C, +50°C, +70°C and +125°C. This approach ensures that the variations of output voltage that occur as the temperature changes within the specified range will be contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale will change from device to device as initial error and the shape of the curve vary. Maximum height of the box for the appropriate temperature range is shown in Figure 8. Duplication of these results requires a combination of high accuracy and stable temperature control in a test system. Evaluation of the AD588 will produce a curve similar to that in Figure 7, but output readings may vary depending on the test methods and equipment utilized.

DEVICE GRADE	MAXIMUM OUTPUT CHANGE – mV 0 TO +70°C	–25°C TO +85°C	–55°C TO +125°C
AD588JQ	2.10		
AD588KQ	1.05		
AD588AD	1.40 (typ)	3.30	
AD588BD	1.05	3.30	
AD588SD			10.80
AD588TD			7.20

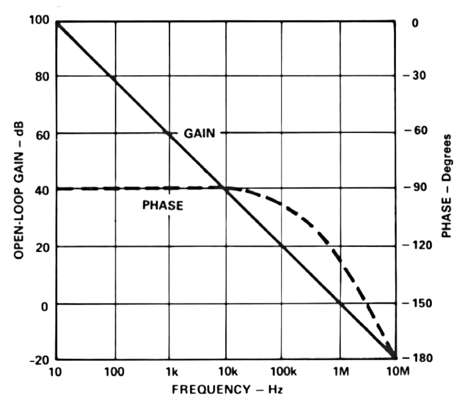
Figure 8. Maximum Output Change—mV

KELVIN CONNECTIONS

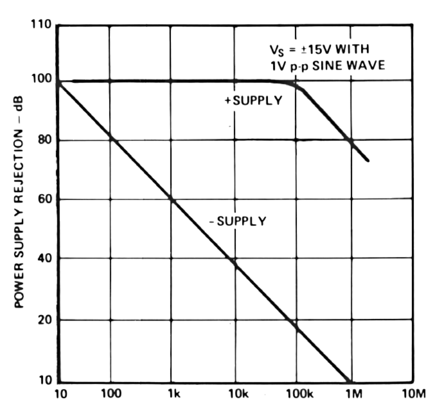
Force and sense connections, also referred to as Kelvin connections, offer a convenient method of eliminating the effects of voltage drops in circuit wires. As seen in Figure 9a, the load current and wire resistance produce an error ($V_{ERROR} = R \times I_L$) at the load. The Kelvin connection of Figure 9b overcomes the problem by including the wire resistance within the forcing loop of the amplifier and sensing the load voltage. The amplifier corrects for any errors in the load voltage. In the circuit shown, the output of the amplifier would actually be at 10 volts + V_{ERROR} and the voltage at the load would be the desired 10 volts.

The AD588 has three amplifiers which can be used to implement Kelvin connections. Amplifier A2 is dedicated to the ground force-sense function while uncommitted amplifiers A3 and A4 are free for other force-sense chores.

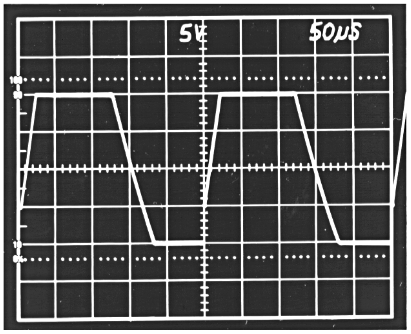
In some single-output applications, one amplifier may be unused.



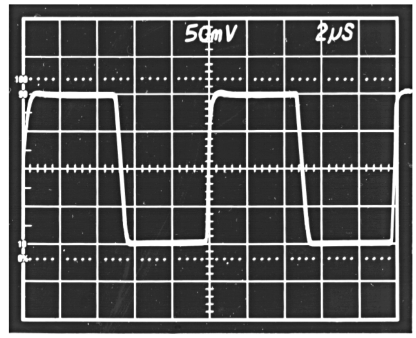
Open Loop Frequency Response (A3, A4)



Power Supply Rejection vs. Frequency (A3, A4)



Unity Gain Follower Pulse Response (Large Signal)



Unity Gain Follower Pulse Response (Small Signal)

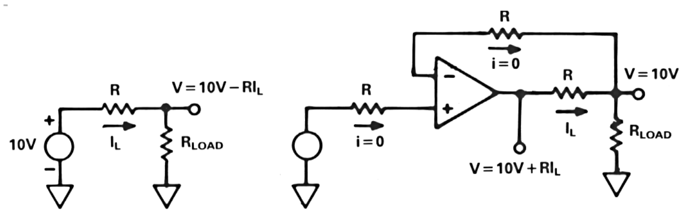
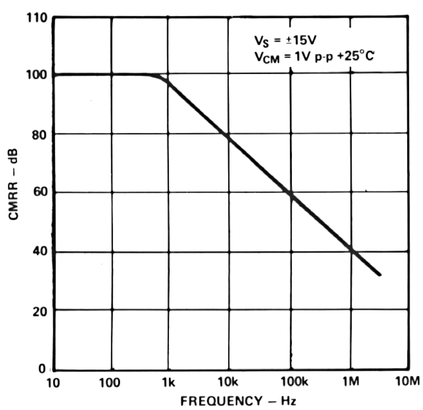


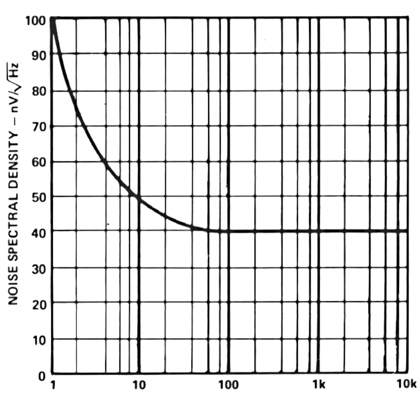
Figure 9. Advantage of Kelvin Connection

In such cases, the unused amplifier should be connected as a unity-gain follower (force + sense pin tied together) and the input should be connected to ground.

An unused amplifier section may be used for other circuit functions as well. The curves on this page show the typical performance of A3 and A4.



Common-Mode Rejection vs. Frequency (A3, A4)



Input Noise Voltage Spectral Density

DYNAMIC PERFORMANCE

The output buffer amplifiers (A3 and A4) are designed to provide the AD588 with static and dynamic load regulation superior to less complete references.

Many A/D and D/A converters present transient current loads to the reference, and poor reference response can degrade the converter's performance.

Figure 10 displays the characteristics of the AD588 output amplifier driving a 0 mA to 10 mA load.

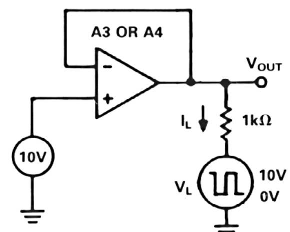


Figure 10a. Transient Load Test Circuit

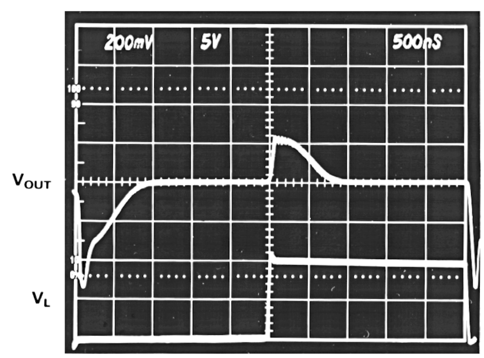


Figure 10b. Large-Scale Transient Response

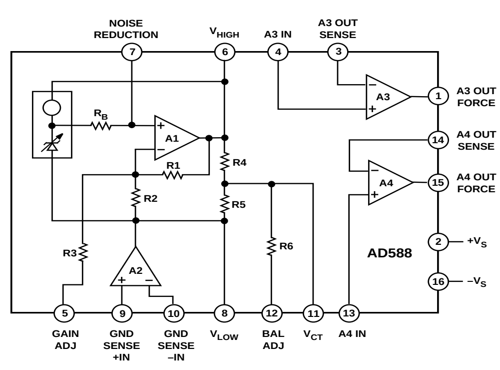


Figure 10c. Fine Scale Settling for Transient Load

Figure 11 displays the output amplifier characteristics driving a 5 mA to 10 mA load, a common situation found when the reference is shared among multiple converters or is used to provide a bipolar offset current.

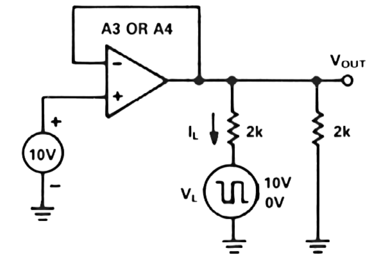


Figure 11a. Transient and Constant Load Test Circuit

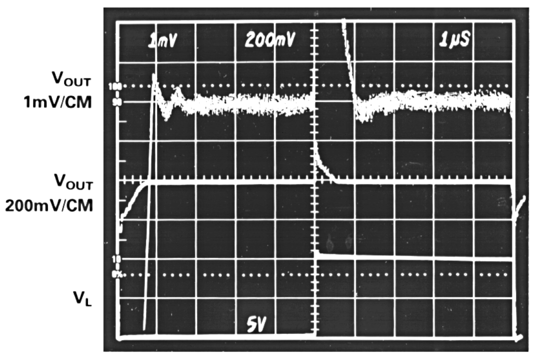


Figure 11b. Transient Response 5 mA–10 mA Load

In some applications, a varying load may be both resistive and capacitive in nature, or be connected to the AD588 by a long capacitive cable.

Figure 12 displays the output amplifier characteristics driving a 1,000 pF, 0 mA-to-10 mA load.

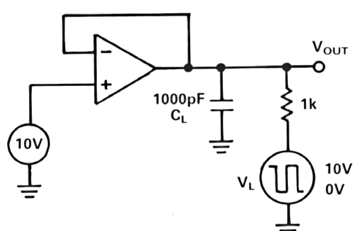


Figure 12a. Capacitive Load Transient Response Test Circuit

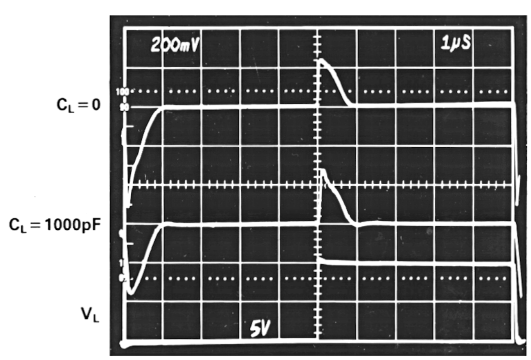


Figure 12b. Output Response with Capacitive Load

Figure 13 displays the crosstalk between output amplifiers. The top trace shows the output of A4, dc-coupled and offset by 10 volts, while the output of A3 is subjected to a 0 mA-to-10 mA load current step. The transient at A4 settles in about 1 μs, and the load-induced offset is about 100 μV.

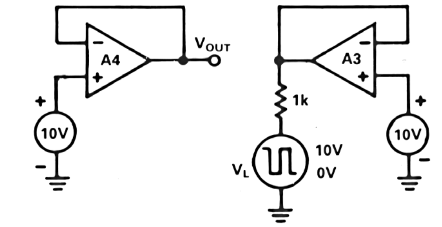


Figure 13a. Load Crosstalk Test Circuit

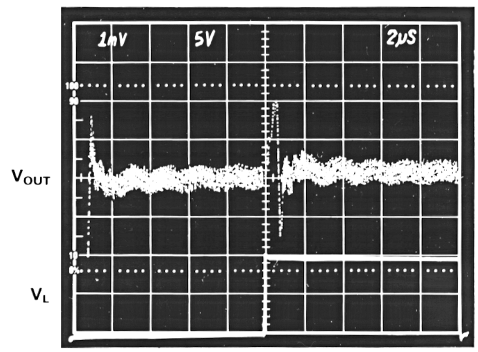


Figure 13b. Load Crosstalk

Attempts to drive a large capacitive load (in excess of 1,000 pF) may result in ringing or oscillation, as shown in the step response photo (Figure 14a). This is due to the additional pole formed by the load capacitance and the output impedance of the amplifier, which consumes phase margin. The recommended method of driving capacitive loads of this magnitude is shown in Figure 14b. The 150 Ω resistor isolates the capacitive load from the output stage, while the 10 kΩ resistor provides a dc feedback path and preserves the output accuracy The 1 μF capacitor provides a high frequency feedback loop. The performance of this circuit is shown in Figure 14c.

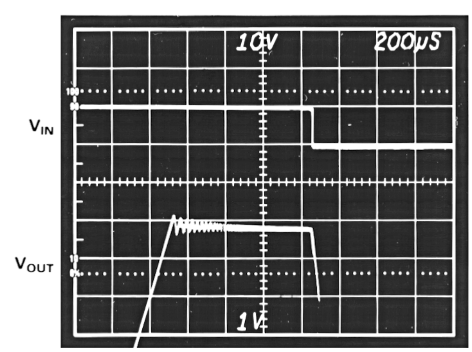


Figure 14a. Output Amplifier Step Response, C_L = 1 μF

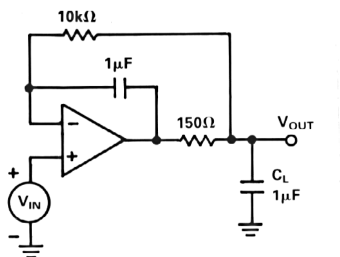


Figure 14b. Compensation for Capacitive Loads

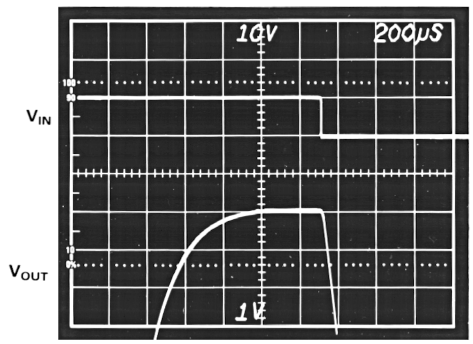


Figure 14c. Output Amplifier Step Response Using Figure 14b Compensation

USING THE AD588 WITH CONVERTERS

The AD588 is an ideal reference for a wide variety of A/D and D/A converters. Several representative examples follow.

14-Bit Digital-to-Analog Converter—AD7535

High resolution CMOS D/A converters require a reference voltage of high precision to maintain rated accuracy. The combination of the AD588 and AD7535 takes advantage of the initial accuracy, drift and full Kelvin output capability of the AD588 as well as the resolution, monotonicity and accuracy of the AD7535 to produce a subsystem with outstanding characteristics.

16-Bit Digital-to-Analog Converter—AD569

Another application which fully utilizes the capabilities of the AD588 is supplying a reference for the AD569, as shown in Figure 16. Amplifier A2 senses system common and forces V_{CT} to assume this value, producing +5 V and –5 V at Pins 6 and 8 respectively. Amplifiers A3 and A4 buffer these voltages out to the appropriate reference force-sense pins of the AD569. The full Kelvin scheme eliminates the effect of the circuit traces or wires and the wire bonds of the AD588 and AD569 themselves, which would otherwise degrade system performance.

SUBSTITUTING FOR INTERNAL REFERENCES

Many converters include built-in references. Unfortunately, such references are the major source of drift in these converters. By using a more stable external reference like the AD588, drift performance can be improved dramatically.

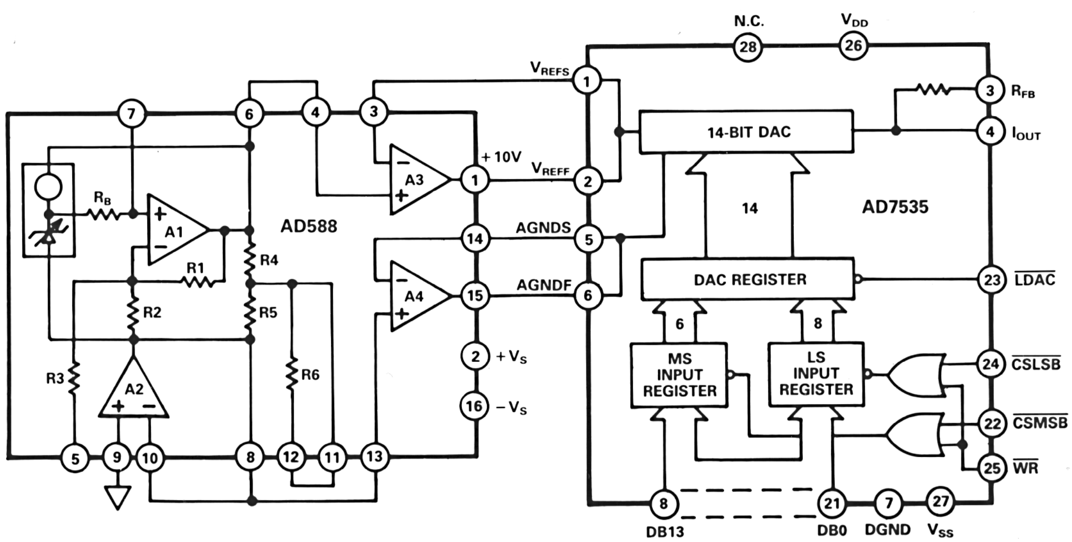


Figure 15. AD588/AD7535 Connections

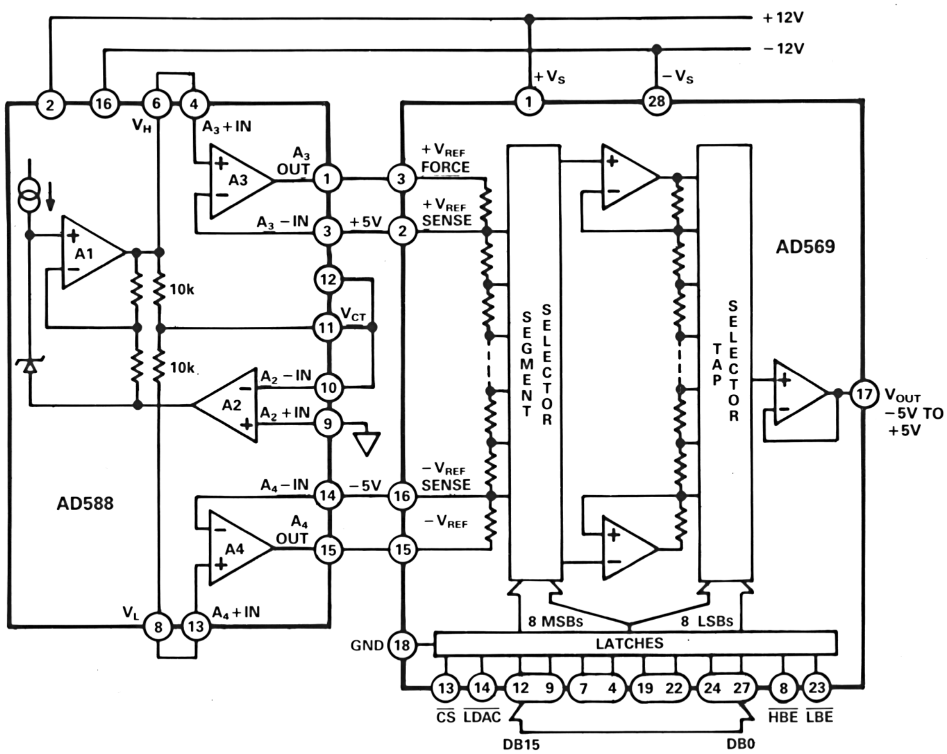


Figure 16. High Accuracy ±5 V Tracking Reference for AD569

12-Bit Analog-to-Digital Converter—AD574A

The AD574A is specified for gain drift from 10 ppm/°C to 50 ppm/°C, (depending on grade) using the on-chip reference. The reference contributes typically 75% of this drift. Therefore, the total drift using an AD588 to supply the reference can be improved by a factor of 3 to 4.

Using this combination may result in apparent increases in full-scale error due to the difference between the on-board reference by which the device is laser trimmed and the external reference with which the device is actually applied. The on-board reference is specified to be 10 V ± 100 mV while the external reference is specified to be 10 V ± 1 mV. This may result in up to 101 mV of apparent full-scale error beyond the ±25 mV specified AD574 gain error. Resistors R2 and R3 allow this error to be nulled. Their contribution to full-scale drift is negligible.

The high output drive capability allows the AD588 to drive up to 6 converters in a multi-converter system. All converters will have gain errors that track to better than ±5 ppm/°C.

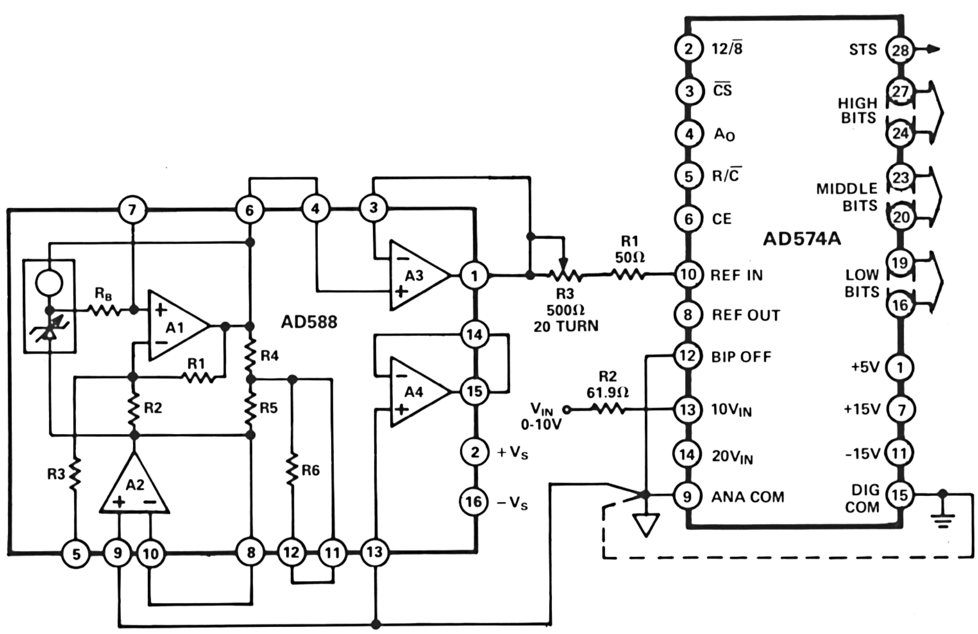


Figure 17. AD588/AD574A Connections

RTD EXCITATION

The Resistance Temperature Detector (RTD) is a circuit element whose resistance is characterized by a positive temperature coefficient. A measurement of resistance indicates the measured temperature. Unfortunately, the resistance of the wires leading to the RTD often adds error to this measurement. The 4-wire ohms measurement overcomes this problem. This method uses two wires to bring an excitation current to the RTD and two additional wires to tap off the resulting RTD voltage. If these additional two wires go to a high input impedance measurement circuit, the effect of their resistance is negligible. Therefore, they transmit the true RTD voltage.

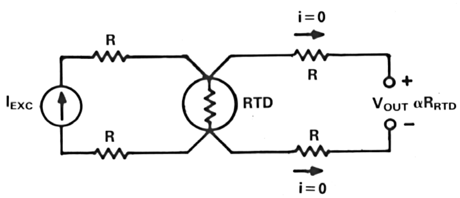


Figure 18. 4-Wire Ohms Measurement

A practical consideration when using the 4-wire ohms technique with an RTD is the self-heating effect that the excitation current has on the temperature of the RTD. The designer must choose the smallest practical excitation current that still gives the desired resolution. RTD manufactures usually specify the self-heating, effect of each of their models or types of RTDs.

Figure 19 shows an AD588 providing the precision excitation current for a 100 Ω RTD. The small excitation current of 1 mA dissipates a mere 0.1 mW of power in the RTD.

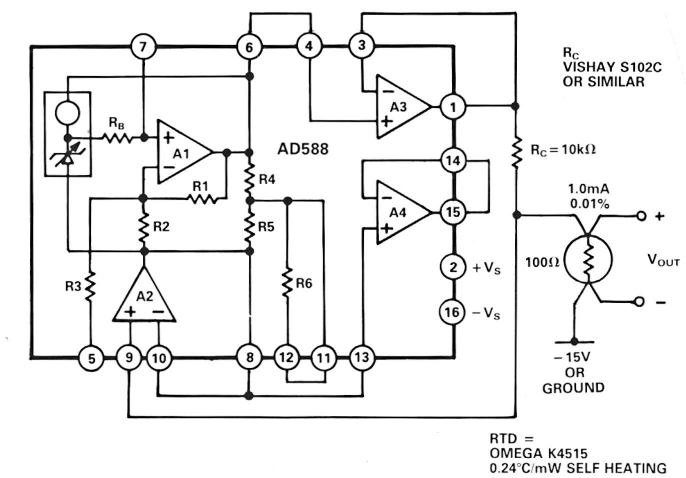


Figure 19. Precision Current Source for RTD

BOOSTED PRECISION CURRENT SOURCE

In the RTD current-source application the load current is limited to ±10 mA by the output drive capability of amplifier A3. In the event that more drive current is needed, a series pass transistor can be inserted inside the feedback loop to provide higher current. Accuracy and drift performance are unaffected by the pass transistor.

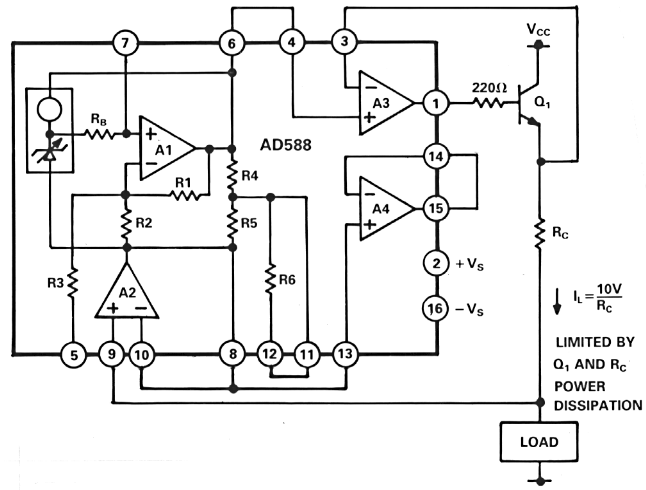
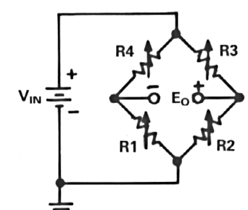


Figure 20. Boosted Precision Current Source

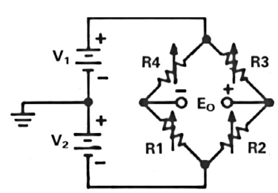
BRIDGE DRIVER CIRCUITS

The Wheatstone bridge is a common transducer. In its simplest form, a bridge consists of 4 two terminal elements connected to form a quadrilateral, a source of excitation connected along one of the diagonals and a detector comprising the other diagonal. Figure 21a shows a simple bridge driven from a unipolar excitation supply. E_O, a differential voltage, is proportional to the deviation of the element from the initial bridge values. Unfortunately, this bridge output voltage is riding on a common-mode voltage equal to approximately $V_{IN}/2$. Further processing of this signal may necessarily be limited to high common-mode rejection techniques such as instrumentation or isolation amplifiers.

Figure 21b shows the same bridge transducer, but this time it is driven from pair of bipolar supplies. This configuration ideally eliminates the common-mode voltage and relaxes the restrictions on any processing elements that follow.



a. Unipolar Drive



b. Bipolar Drive

Figure 21. Bridge Transducer Excitation

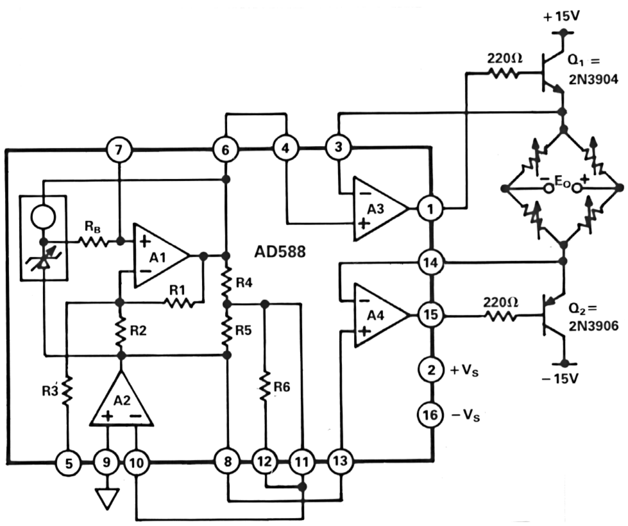


Figure 22. Bipolar Bridge Drive

As shown in Figure 22, the AD588 is an excellent choice for the control element in a bipolar bridge driver scheme. Transistors Q1 and Q2 serve as series pass elements to boost the current drive capability to the 28 mA required by a typical 350 Ω bridge. A differential gain stage may still be required if the bridge balance is not perfect. Such gain stages can be expensive.

Additional common-mode voltage reduction is realized by using the circuit illustrated in Figure 23. A1, the ground sense amplifier, servo's the supplies on the bridge to maintain a virtual ground at one center tap. The voltage which appears on the opposite center tap is now single-ended (referred to ground) and can be amplified by a less expensive circuit.

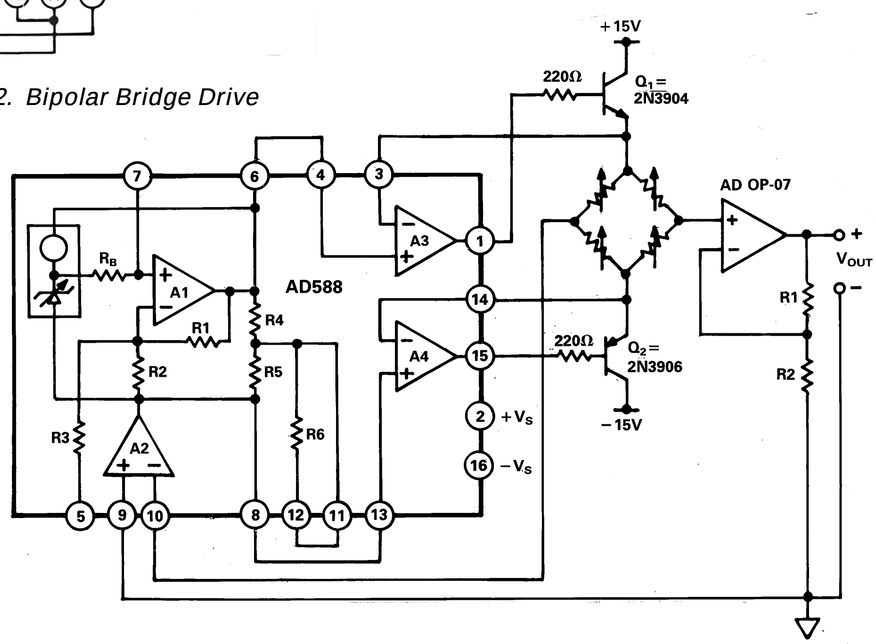
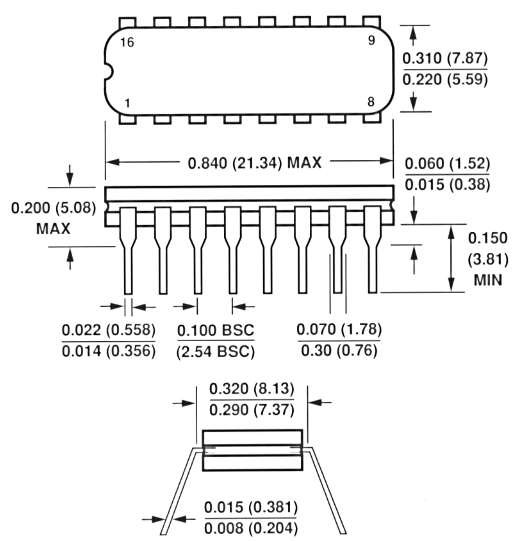


Figure 23. Floating Bipolar Bridge Drive with Minimum CMV

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Cerdip (Q) Package



C1016b–10–10/86

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